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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/583,233	05/31/2000	Tomomi Furudate	P108397-00011	3618

7590 07/09/2003

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EXAMINER
HO, THANG H

ART UNIT	PAPER NUMBER
2188	4

DATE MAILED: 07/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/583,233	FURUDATE ET AL.	
	Examiner	Art Unit	
	Thang H Ho	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *360579* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 360579, filed on 12/20/1999.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 5-7 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Imura et al. (USPN 5,398,212).

As per claim 5, Imura discloses in figure 1 a semiconductor memory device comprising a plurality of memory cells (3), an invalid address detecting circuit (5) for detecting address signal supplied from exterior indicating an address space other than the address space, and an output controlling circuit (6) which can be programmed to output, when the invalid address detecting circuit carries out detection in a read operation, a data signal read in a read operation cycle immediately preceding a read operation (e.g. see column 6, lines 52-54).

As per claim 6, Imura further discloses in figure 5 an output circuit for receiving a read data signal from memory cells (3) and continuously outputting the received data to

the exterior, according to a control by the output controlling circuit (6) when the invalid address detecting circuit carries out detection in the read operation.

As per claim 7, Imura discloses in figure 1 a semiconductor memory device comprising a plurality of memory cells including nonvolatile memory devices (e.g. see figure 1, element 3 and column 5, lines 17-25), a command controlling circuit (6), and an invalid address detecting circuit (5) for detecting that an address signal supplied from exterior as the command input indicates an address space other than the address space, wherein the command input is invalidated when the invalid address detecting circuit carries out detection. Imura does not disclose the command controlling circuit for accepting and validating command control inputs specifically neither in controlling a write nor an erase operation. However, it is well known in the art of flash memory that a flash memory device is an electrically write-able and erasable device and it is capable of accepting a write and erase command. It is inherent that, in order to implement the semiconductor memory device utilizing flash memory, the command control circuit would need to be modified or reprogrammed to carry out a write and erase operation.

As per claim 10, it encompass the same scope of invention as to that of claim 7 above, however it is drafted as method format rather than apparatus format, the claim is therefore rejected for the same reasons as being set forth above.

Accordingly, Imura anticipated the claimed invention.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imura et al. (USPN: 5,398,212), hereinafter Imura; in view of Howard (USPN: 5,754,816).

As per claims 1, Imura teaches the device as claimed including a semiconductor memory device in figure 6 comprising: a plurality of memory cells (3) corresponding to an address space larger than 2^n and smaller than $2^{(n+1)}$, where n is a positive integer; and an invalid address detecting circuit (5) for detecting that an address signal supplied from exterior indicates an address space other than the address space.

Imura does not teach the invalid signal outputting circuit for outputting an invalid signal to the exterior when the invalid address detecting circuit carries out the detection.

Howard teaches in figure 1 the usage of an invalid signal outputting circuit (12) for outputting invalid signal to provide the status of the memory accessing operation and to control the output circuit; turning on the output circuit only when the valid access signal is asserted true (e.g. see figure 2, and column 4, lines 7-20).

Accordingly, it would have been prima facie obvious for one skilled in the art at the time the invention was made to implement a semiconductor memory device as taught by Imura and modify the device to include an invalid signal outputting circuit as taught by Howard to generate the claimed invention with a reasonable expectation of success. One skilled in the art would have been motivated to do so because it would reduce power consumption by preventing invalid address from propagating to the output circuit and to provide the status of the memory access to interfacing devices.

As per claim 2, Imura discloses in figure 6 the device as in claim 1 comprising an output controlling circuit (7) for outputting, when the invalid address detecting circuit carries out the detection in a read operation, a data signal read in a read operation cycle immediately preceding the read operation.

As per claim 3, Imura discloses in figure 6 the device as in claim 2 comprising an output circuit (4) for receiving a read data signal from the memory cells (3) and continuously outputting the received data to the exterior, according to a control by the output controlling circuit (7) when the invalid address detecting circuit carries out the detection in the read operation.

As per claim 4, Imura discloses the outputting of high impedance when the invalid address detecting circuit detects an invalid address in a read operation (e.g. see table 2, column 8, lines 57 et seq.).

As per claim 8, Imura discloses the device as in claim 7 as applied to claim 1 above comprising an invalid signal outputting circuit for outputting an invalid signal to the exterior when the invalid address detecting circuit carries out said detection.

As per claim 9, it encompass the same scope of invention as to that of claims 1-4 above, however it is drafted as method format rather than apparatus format, the claim is therefore rejected for the same reasons as being set forth above.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

After-final	(703) 746-7238
Official	(703) 746-7239
Non-Official/Draft	(703) 746-7240

Hand–delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA. Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thang H Ho whose telephone number is 703-305-1888. The examiner can normally be reached on Monday-Friday from 7:00 A.M. - 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-6606 for regular communications and 703-308-9051 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

TH
July 7, 2003

Kevin L. Ellis
Primary Examiner